Instruction manual

USE This Book For CPU Only !!

DATA I/O

Programming systems for tomorrow... today

PROM PROGRAMMER

Program Card Set

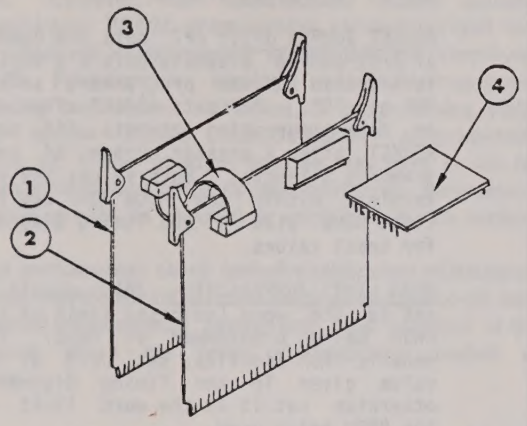
C25-1286-1

REV G JULY 78

909-1286-1

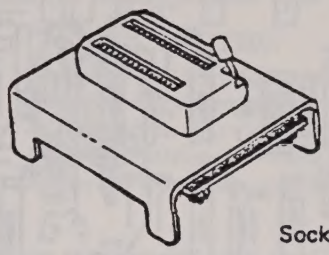
Page 2 of 3 of Cal Sheet
Revised: 12/1/81
RDH.

SPECIFICATION



1. Digital Card	701-1225
2. Analog Card	701-1286
3. Interconnect Cable	709-1608
4. Calib. Program Adapter	910-1286

Fig. 1-1. Program Card Set 909-1286



Socket Adapter

DESCRIPTION

Program (Personality) Card Set 909-1286-1, with the appropriate Socket Adapter, provides Data I/O PROM programmers with the capability of programming and reading the PROMs listed in Table 1-1. Socket Adapters are available for each PROM listed. Table 1-1 references the Socket Adapters required to program (or read) the various PROMs.

INSTALLATION

Turn power OFF while changing Card Sets. Install the Digital Card in programmer Brown-Orange card slot; install the interconnected Analog Card in White-White card slot. Component sides of cards should face forward in programmer Models 1-5, to the right in programmer satellites and down in programmer Models 7 and 9. Connect J2 on Analog Card to front panel Socket Receptacle. Refer to the programmer manual for more detailed installation instructions.

CALIBRATOR PROGRAM ADAPTER

Program Card Set 909-1286-1, includes Calibrator Program Adapter 910-1286-1, which mates with the Data I/O Universal Calibrator. As shipped, this Program Card Set is precalibrated according to Data I/O Calibration Procedure 017-1286-1, which is included in the Performance Check Section of this manual.

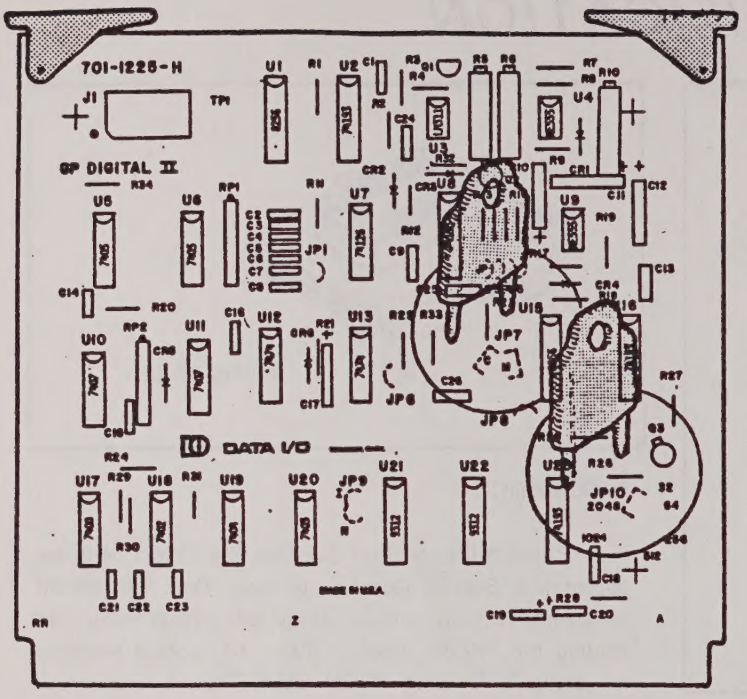
CALIBRATION AND PERFORMANCE CHECK

Card Set calibration and performance verification procedures are given in the following pages. Calibration should be performed every 90 days, or if PROM programming yields fall below PROM manufacturers' recommendations. Performance Check should be performed after each calibration.

Table 1-1. PROM types to Data I/O Socket Adapters.

Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
ADVANCED MICRO DEVICES				
32x8 FL	27S08/LS08	VOL OC	16 PIN	1407-2
32x8 FL	27S09/LS09	VOL TS	16 PIN	1407-2
32x8 FL	27S18	VOH OC	16 PIN	1407-1
32x8 FL	27S19	VOH TS	16 PIN	1407-1
256x4 FL	27S10	VOL OC	16 PIN	1408-3
256x4 FL	27S11	VOL TS	16 PIN	1408-3
256x4 FL	27S20	VOH OC	16 PIN	1408-1
256x4 FL	27S21	VOH TS	16 PIN	1408-1
512x4 FL	27S12	VOH OC	16 PIN	1408-2
512x4 FL	27S13	VOH TS	16 PIN	1408-2
512x8 FL	27S15	VOH TS	24 PIN	1411-1
512x8 FL	27S26	VOH OC	22 PIN	1412-2
512x8 FL	27S27	VOH TS	22 PIN	1412-2

4032583-15 27S15
403796-423 27S19

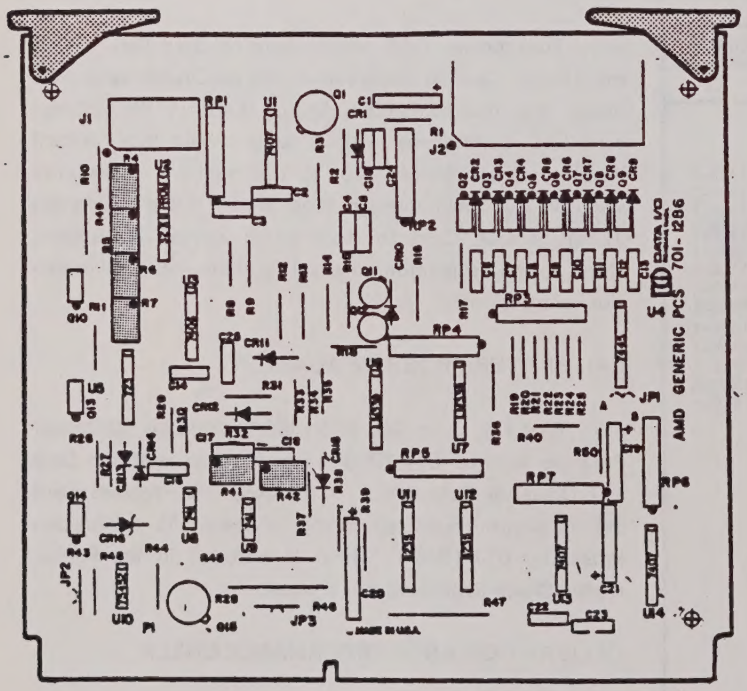


JUMPER POSITIONS, DIGITAL CARD

REJECT JUMPER JP7: JP7 sets the number of programming attempts before a REJECT is signaled to the programmer; select "M" or "C". "M" sets REJECT after one or more programming attempts; "C" sets REJECT after a greater number of programming attempts. Both values are determined within the Mode ROM. See the right hand side of the Timing Diagram* for exact values.

WORD LIMIT JUMPER JP10: JP10 should be set to the word (address) limit of the PROM being programmed or read. For generic PROM families, set JP10 at the value given in the Timing Diagram*, otherwise set it at the word limit of the PROM being used.

* The Timing Diagram is located with the schematics, at the rear of this manual.



ADJUSTMENT LOCATIONS, ANALOG CARD

Adjustment locations are shown shaded. These adjustments are made during Calibration, as explained in the following section.

INTRODUCTION

Since PROM manufacturers' shipments can vary from lot to lot, slight variations in PROM programming yields are to be expected. However, each manufacturer usually specifies certain minimum PROM programming yields—provided that specific approved programming techniques are employed. Data I/O Programmers employ manufacturer-approved programming techniques: therefore, if programming yields diminish below PROM manufacturers' recommended minimums, or, if the program card set has been in use for more than ninety days since its last calibration, programmer performance should be checked as explained in this section.

The performance check includes calibration adjustments of program waveform amplitudes and includes go/no-go tests of all critical programming parameters. Also included in the performance check are tests on resistively loaded ac waveforms.

DATA I/O FIELD SERVICES

Data I/O, Inc. furnishes complete programmer repair and calibration services at regional Field Service Centers and at the Data I/O factory. Contact your local Data I/O representative for further information.

TEST EQUIPMENT REQUIRED

To perform a complete performance check, the following equipment is required:

1. Data I/O Universal Calibrator, P/N 910-1071.

2. A. Prog. 1, 2, 3, 5: Data I/O Extender Card, P/N 910-1136.
   B. Prog. 9: Data I/O Extender Fixture, P/N 910-1074.

3. Digital Voltmeter: Fluke Model 8000A, or equivalent

4. Adjustment Tool: A three-inch screwdriver

5. Dual Trace Oscilloscope: Tektronix 465, or equivalent

6. Programmers 1, 2, 3, 5 only: Data I/O 13 inch Interconnect Cable, P/N 709-1613.

7. Programmer 9 only: Data I/O Interconnect Cables, P/N 709-1613 and 709-2608.

8. Jumper wires approximately 12 inches in length.

INSTALLATION OF UNIVERSAL CALIBRATOR

The following installation procedure assumes that the Universal Calibrator is mated with the Extender Card and that programmer power is off. On Programmers 1, 2, 3, and 5, remove the top cover to expose the card cage. To expose the card cage on the Model 9, open the access opening on the front of the chassis.

1. Remove end of 26-conductor cable from analog card. Remove both cards (analog and digital) from Programmer (or Satellite) card cage.

2. Remove end of 16 conductor cable from digital card J1.

CAUTION

Connector pins are fragile; careless connector extraction may result in bent or broken pins. Use a suitable tool--like a small screwdriver--when removing connectors from their sockets.

3. Install the extender card (with the Universal Calibrator in place).
   A. Programmers 1-5: Install the extender card into the analog card slot (white-white).
   B. Programmer 9: Install extender fixture into digital card slot (brown- orange).

4. A. Programmers 1-5: Install the analog card of the program card set into the card slot on top of the extender board. Refer to Figure 1.
   B. Programmer Model 9: Install the analog card in front card slot. Refer to Figure 2. The components should face the Calibrator.

5. A. Programmers 1-5: Install the digital card in the digital slot in the programmer.
   B. Programmer 9: Install the digital card behind the analog card on top of the extender card.

6. Making sure that cable red stripes and connector pins 1 are properly oriented, connect the analog card to the Universal Calibrator as follows:
   A. Programmers 1-5: Connect J1 of the analog card to J1 of the Universal Calibrator using the strap between the analog and digital cards. Connect J2 of the analog card to J2 of the Universal Calibrator using the ribbon cable that connects the card set and the programmer.
   B. Programmer 9: Connect J1 of the analog card to J1 of the Universal Calibrator using the strap between the analog and digital cards. Using the 26-connector cable supplied with the Calibrator, connect J2 of the analog card to J2 of the Calibrator.

7. Plug Calibrator Program Adapter into PROGRAM ADAPTER SOCKET on Universal Calibrator.

CAUTION

Be sure that the four-digit portions of both part numbers are identical: i.e. Analog card 701-XXXX is part of program card set 909-XXXX, which is calibrated by calibrator program adapter 910-XXXX.

8. Connect DVM ground probe to GND test point at left side of Universal Calibrator.

This completes installation of the Universal Calibrator.

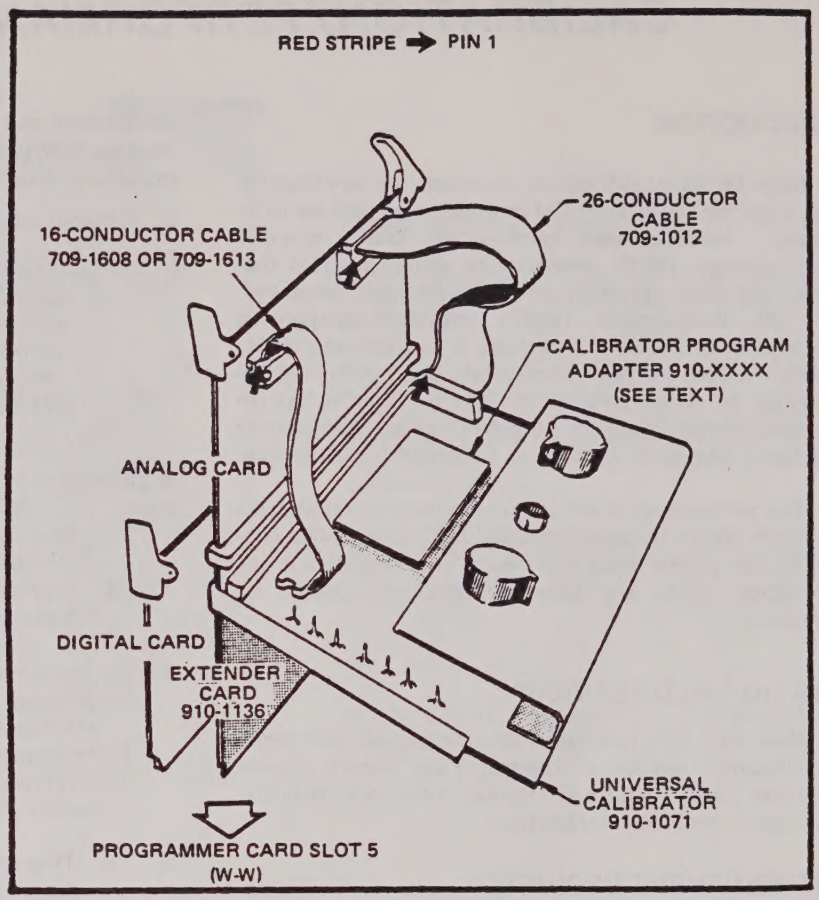


Figure 1. Installation of Universal Calibrator into Programmer Models 1, 2, 3, and 5 for Calibration/Performance Check.

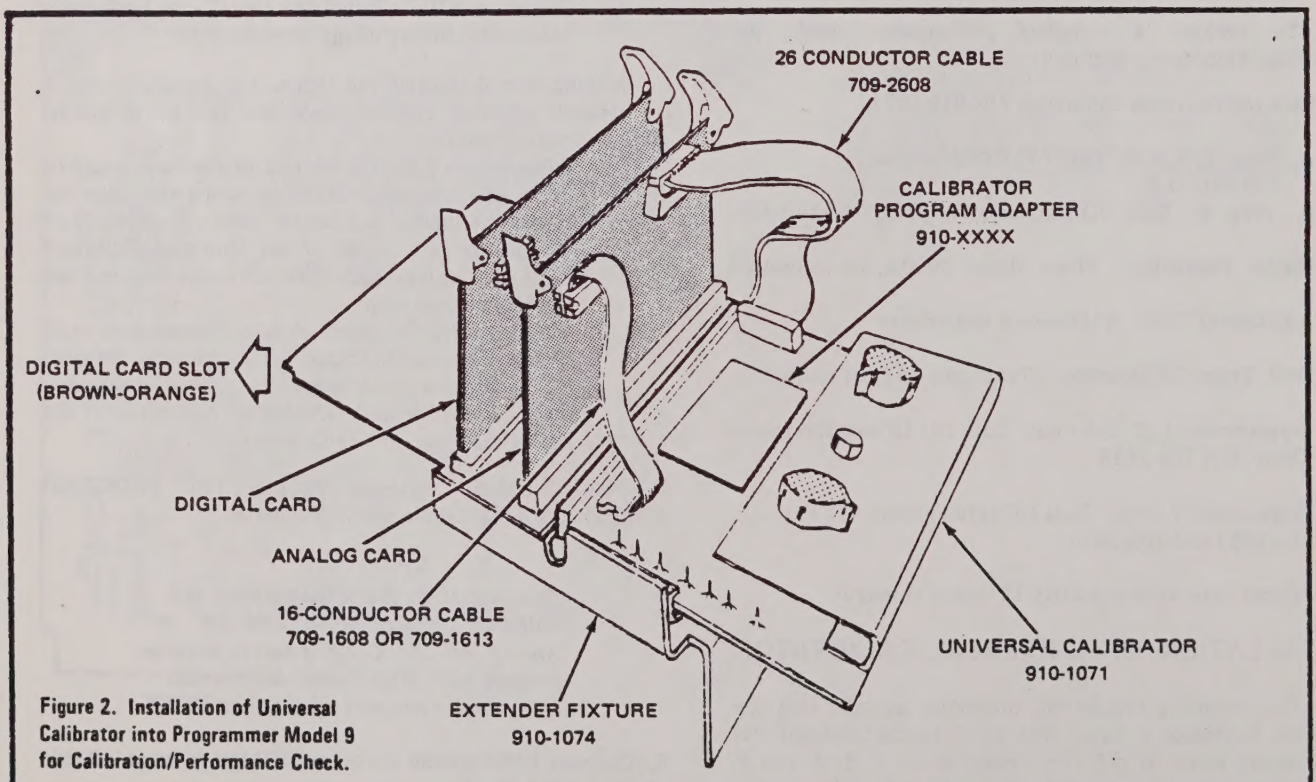


Figure 2. Installation of Universal Calibrator into Programmer Model 9 for Calibration/Performance Check.

CALIBRATION CHART

The calibration chart is to be used only with the (calibrator) program adapter specified in the title block of the chart.

The left-most portion of the chart contains truth tables for the calibrator program adapter. The truth tables are for documentation purposes only, and have no bearing on the actual performance check/calibration procedures.

PROGRAMMER WORD COUNT COLUMN is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When using the chart, refer to the address (word count) corresponding to the address readout configuration of the programmer in use. For instance, if your programmer has a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static (DC steady state) conditions created by the Universal Calibrator may cause thermal damage to compo-components if Programmer is left unattended with advanced word count.

TEST DESCRIPTION column contains three kinds of tests: (1) power supplies, (2) performance checks, and (3) calibration adjustments. The power supply tests are contained in the first five rows of the chart. (Note that power supply adjustments are located in the programmer, not in the program card set.) Performance checks fill the bulk of the Calibration Chart; these are characterized by min/max voltage limits only. No nominal (NOM) values are given, and no adjustments (ADJ) are prescribed.

Calibration steps are those with entries in the ADJ and NOM columns. These steps are evident by the note "CALIBRATION STEP" in the comments column.

SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load select switch; S3 is the line select switch. Generally, each step on the Calibration Chart requires changing of switch positions. S1 is push to test, and should be held depressed only long enough to obtain a DVM reading.

CAUTION

DO NOT hold S1 depressed for extended periods. Certain measurements induce high Programmer current levels. Extended high current operation (S1 depressed) may damage sensitive electronic components.

TEST POINT column gives test point location for DVM probe on Universal Calibrator. Some test points are located on the program card itself; for instance, if a test point is designated as U6 P8, it means that the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the comments column.

The ADJ column calls out potientiometer designations. The first four entries in the ADJ column refer to power supply potientiometers located on the power supply board of the Programmer. If adjustments are required, refer to Programmer manual. The remaining entries in the ADJ column refer to pots on the analog card. These are located as shown on page 1-2 in the Specifications section of this manual.

The LIMITS COLUMN is divided into three portions: MIN (minimum), NOM (Nominal), and MAX (Maximum). The values given are in volts, and indicate the range into which a given DVM reading should fall when S1 is pressed. If a reading is within the limits, no adjustment is required and the programmer (or program card set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (calibration steps), the card is non functional and should not be used for programming.

NOTES are written in a block at the bottom of the calibration chart. These apply to certain calibration steps and are referenced by numbers in the comments column. Notes called out by letter in the comments column apply only to Model IX calibration.

PERFORMANCE CHECK AND CALIBRATION PROCEDURE

DC CALIBRATION

The following paragraphs describe the method by which a program card set is checked/calibrated in conjunction with the applicable Calibration Chart. The procedure assumes that the Universal Calibrator is properly installed, as previously described. The following procedure should be performed with the programmer in an ambient temperature range between 15°C to 35°C.

Initialization

1. Switch Programmer power ON; allow Programmer to warm up for approximately five minutes.
2. Programmers 1, 2, 3, and 5:
   Press: RESET
   ROM2-ROM2
   MANUAL
   PROGRAM
   START

   Programmer 9:
   Press: EXECUTE
   Set NORMAL/INVERT switch to INVERT. .

Power Supply

During the procedure the programmer card cage should contain all boards normally used.

Connect DVM between GND and the Universal Calibrator test points given in Steps 1-1 through 1-5 on the Calibration Chart. Measured voltages should fall within the given limits. (Calibrator Switch positions do not matter.)

If any power supply voltage measurement reading is outside of the given range, adjustment must be made. Power supply adjustments are located on the power supply board within the Programmer.

If a Programmer Satellite is being used, check/calibrate Satellite power supply as explained in Satellite Manual.

Performance Check/Calibration

1. Use FWD and REV keys on Programmer keyboard to index the "address display" (word count) to the decimal (DEC), hexadecimal (HEX), or octal (OCT) address given in the word count column of the calibration chart.

CAUTION

DO NOT leave Word Count advanced beyond 000 for extended periods. Static (DC steady state) conditions created by the Universal Calibrator may cause thermal damage to components if Programmer is left unattended with advanced word count. Press Reset to relieve possible thermal stresses.

2. With Word Count set, and DVM probes installed between GND and the indicated test point on the universal calibrator, set switches S2 and S3 to the positions indicated. Press S1 to test.

CAUTION

DO NOT hold S1 depressed for extended periods. Certain measurements induce high current levels within the Programmer. Extended high current operation (S1 depressed) puts unnecessary stress on sensitive electronic components.

3. While S1 is held, DVM readings should fall between the indicated limits for each measurement. If a DVM reading is outside of limits, or if the reading cannot be adjusted to fall within limits (ADJ column), DO NOT use the card set for programming.

Proceed through the Calibration Chart until all tests have been performed. At the conclusion of testing, turn Programmer power OFF, and proceed to AC Dynamic Tests.

AC CALIBRATION

AC Dynamic Tests

The following procedure is used to obtain the "Program Waveforms" shown on the Timing Diagram at the rear of this manual.

These waveforms, indicated by circled digits (①,②,③,..) on the timing diagram, are identically referenced on the Calibration Chart. The waveforms are obtained by selecting switch positions (S2 and S3) on the Universal Calibrator and feeding the selected signals to an appropriately triggered dual trace oscilloscope.

Test Set-Up

1. Make sure that programmer power is Off.

2. A. Programmers 1-5: Remove the digital card from the card cage. Refer to Figure 3.
   B. Programmer 9: Remove the digital card from the extender. Refer to Figure 4.

3. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

4. A. Programmers 1-5: Disconnect the other end of the 16-conductor cable from J1 of the analog card. Substitute the 13 inch cable supplied with the Calibrator, and connect J1 of the analog card to J1 of the digital card.
   B. Programmer 9: Connect the free end of the 16-conductor cable to digital card J1, assuring that cable red stripe and connector pin 1 are properly oriented.

5. Connect triggered input channel of dual trace oscilloscope to digital card test pulse. The location of the test pulse on the digital card is noted to the left of the Test waveform on the digital card. Connect the other channel to TP3 on the Calibrator. Re-install the digital card per step 2, above.

6. Using a suitable jumper cable, connect the Read Enable line emanating from analog card J1-16 to ground. (Use either the programmer chassis or the GND test point on the Universal Calibrator.)

7. Programmer 9: Set NORMAL/INVERT switch to INVERT.

CAUTION

Make sure that J1-16 is properly connected to ground. If it is inadvertently connected to any other potential, damage to Programmer components may result.

8. Turn Programmer power ON.

9. Programmers 1, 2, 3, 5:
   Press: RESET
   RAM-RAM
   PROGRAM
   MANUAL
   START
   Programmer 9:
   Press: KEYBOARD

Calibration Chart

DATA I/O
Programming systems for tomorrow...today

CALIBRATION CHART 017-1286-1 PROGRAM CARD 909-1286-1
FIXTURE 702-1071 MANUFACTURER A.M.D.
PROGRAM ADAPTER 910-1286-1 PROM GENERIC FAMILY

DATE	REV	REVISION RECORD	DR	CK
5-78	D	CN #2230	KL	KJ
6-78	E	CN #2308	KJ	RT
7-78	F	CN #2332	KJ	RT
4-79	–	CN #2565	FS	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	COMMENTS
44	0A	+24	1-1	000	00	000			+24	R26	23.5	24.0	24.5	Adjustments are located on the power supply board. See programmer manual.
44	0A	POWER +48	1-2	000	00	000			+48	R24	49.4	49.7	49.8	
44	0A	SUPPLIES +5	1-3	000	00	000			+5	R18	5.05	5.1	5.15	
44	0A	-9	1-4	000	00	000			-9	R40	-9.2	-9.0	-8.8	
44	0A	PROGRAMMABLE SUPPLY	1-5	000	00	000			PROG V		27.0		29.0	
44	0A	VCC VERIFY VL	2-0	000	00	000	5	1	TP3	R6	4.00	4.25	4.50	*Adjustment Step.*
44	0E	VCC VERIFY VH	2-1	001	01	001	5	1	TP3	R5	4.75	5.00	5.25	*Adjustment Step.*
44	06	VCC READ	2-2	002	02	002	5	1	TP3	R4	4.75	5.00	5.25	*Adjustment Step.*
64	03	VCC PROGRAM (1)	2-3	003	03	003	5	1	TP3	R7	5.00	5.25	5.50	*Adjustment Step.*
64	03	VCC CURRENT ICC	2-4	003	03	003	6	1	TP3		5.0		8.0	
64	03	VCC KILL	2-5	003	03	003	5	1	TP3		0.0		0.4	Set programmer in STOP.
64	03	VERIFY REFERENCE	3-1	003	03	003			U7 P8		1.6		1.8	Test point located on analog card.
64	03	VERIFY LOAD IN	3-2	003	03	003	3	8	TP3		1.8		2.6	
64	04	VERIFY LOAD OUT	3-3	004	04	004	7	8	TP3		0.0		1.0	
64	04	$\overline{CE}$ PROGRAM (2)	4-1	004	04	004	3	5	TP3	R41	14.5	15.0	15.5	*Adjustment Step.*
64	0E	$\overline{CE}$ DISABLE	4-2	005	05	005	7	5	TP3		3.5		4.5	
64	0F	$\overline{CE}$ VERIFY	4-3	006	06	006	7	5	TP3		0.0		0.4	
64	0F	CP LOW LEVEL (6)	4-4	006	06	006	7	6	TP3		0.0		0.4	
64	16	CP HIGH LEVEL	4-5	007	07	007	7	6	TP3		4.8		5.15	
64	E4	BIT 8 PROGRAM V OUT SET	5-1	008	08	010	5	8	TP3	R42	19.5	20.0	20.5	*Adjustment Step.*
64	C4	BIT 8 NO PROGRAM	5-2	009	09	011	7	8	TP3		0.0		1.0	
64	C4	BIT 7 PROGRAM	5-3	009	09	011	5	9	TP3		19.5		20.5	
64	A4	BIT 7 NO PROGRAM	5-4	010	0A	012	7	9	TP3		0.0		1.0	
64	A4	BIT 6 PROGRAM	5-5	010	0A	012	5	10	TP3		19.5		20.5	
64	84	BIT 6 NO PROGRAM	5-6	011	0B	013	7	10	TP3		0.0		1.0	
64	84	BIT 5 PROGRAM	5-7	011	0B	013	5	11	TP3		19.5		20.5	
64	64	BIT 5 NO PROGRAM	5-8	012	0C	014	7	11	TP3		0.0		1.0	
64	64	BIT 4 PROGRAM	5-9	012	0C	014	5	12	TP3		19.5		20.5	
64	44	BIT 4 NO PROGRAM	5-10	013	0D	015	7	12	TP3		0.0		1.0	

COMMENTS
- Use paragraphs 4.3.1-4.3.5 for key sequences for COMMENTS below.
- Switch S1 must be depressed for accurate readings.
- CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	CALIBRATION CHART 017-1286-1 PAGE 2 OF 3
64	44	BIT 3 PROGRAM	5-11	013	0D	015	5	23	TP3		19.5		20.5	
64	24	BIT 3 NO PROGRAM	5-12	014	0E	016	7	23	TP3		0.0		1.0	
64	24	BIT 2 PROGRAM	5-13	014	0E	016	5	22	TP3		19.5		20.5	
64	04	BIT 2 NO PROGRAM (4)	5-14	015	0F	017	7	22	TP3		0.0		1.0	
64	04	BIT 1 PROGRAM (3)	5-15	015	0F	017	5	21	TP3		19.5		20.5	
64	E4	BIT 1 NO PROGRAM	5-16	016	10	020	7	21	TP3		0.0		1.0	
64	E4	BIT CURRENT LIMIT IOP	5-17	016	10	020	6	8	TP3		4.0		6.0	
C4	07	BIT 8 COMPARATOR	6-1	017	11	021	5	8						Confirm bits 1 - 7 ON (HEX 7F) on DO Bus.
C4	07	BIT 7 COMPARATOR	6-2	017	11	021	5	9						Confirm bits 1 - 6 and 8 ON (HEX BF) on DO Bus.
C4	07	BIT 6 COMPARATOR	6-3	017	11	021	5	10						Confirm bits 1 - 5, 7 and 8 ON (HEX DF) on DO Bus.
C4	07	BIT 5 COMPARATOR	6-4	017	11	021	5	11						Confirm bits 1 - 4 and 6 - 8 ON (HEX EF) on DO Bus.
C4	07	BIT 4 COMPARATOR	6-5	017	11	021	5	12						Confirm bits 1 - 3 and 5 - 8 ON (HEX F7) on DO Bus.
C4	07	BIT 3 COMPARATOR	6-6	017	11	021	5	23						Confirm bits 1, 2 and 4 - 8 ON (HEX FB) on DO Bus.
C4	07	BIT 2 COMPARATOR	6-7	017	11	021	5	22						Confirm bits 1 and 3 - 8 ON (HEX FD) on DO Bus.
C4	07	BIT 1 COMPARATOR	6-8	017	11	021	5	21						Confirm bits 2 - 8 ON (HEX FE) on DO Bus.
C4	07	VOH DETECT	6-9	017	11	021	7	7						Confirm all bits ON (HEX FF) on DO Bus. *
C4	07	VOL DETECT	6-10	017	11	021	5	7						Confirm all bits OFF (HEX 00) on DO Bus. *
44	07	READ ENABLE	6-11	018	12	022	7	7						Confirm all bits OFF (HEX 00) on DO Bus.
C0	07	GROUND TEST	7-1	019	13	023	8	24	TP3		0.0		0.08	
64	A4	ADDRESS TEST A0 VIL (5)	8-1	682	2AA	1252	7	20	TP3		0.0		0.4	
64	A4	ADDRESS TEST A1 VIH	8-2	682	2AA	1252	7	19	TP3		4.8		5.15	
64	A4	ADDRESS TEST A2 VIL	8-3	682	2AA	1252	7	18	TP3		0.0		0.4	
64	A4	ADDRESS TEST A3 VIH	8-4	682	2AA	1252	7	17	TP3		4.8		5.15	
64	A4	ADDRESS TEST A4 VIL	8-5	682	2AA	1252	7	16	TP3		0.0		0.4	
64	A4	ADDRESS TEST A5 VIH	8-6	682	2AA	1252	7	15	TP3		4.8		5.15	
64	A4	ADDRESS TEST A6 VIL	8-7	682	2AA	1252	7	14	TP3		0.0		0.4	
64	A4	ADDRESS TEST A7 VIH	8-8	682	2AA	1252	7	13	TP3		4.8		5.15	
64	A4	ADDRESS TEST A8 VIL	8-9	682	2AA	1252	7	2	TP3		0.0		0.4	
64	A4	ADDRESS TEST A9 VIH	8-10	682	2AA	1252	7	3	TP3		4.8		5.15	
64	A4	ADDRESS TEST A10 VIL	8-11	682	2AA	1252	7	4	TP3		0.0		0.4	
64	04	ADDRESS TEST A0 VIH	8-12	1365	555	2525	7	20	TP3		4.8		5.15	
64	04	ADDRESS TEST A1 VIL	8-13	1365	555	2525	7	19	TP3		0.0		0.4	

* ON SYS 19 6-9 Comments: OK
6-10 " : S/B Confirm all bits on (HEX FF) on DO Bus
6-11 " : OK
Add: 6-12 word 12, S2=5, S3=7
Comments: Confirm all bits ON (HEX FF) on DO Bus.

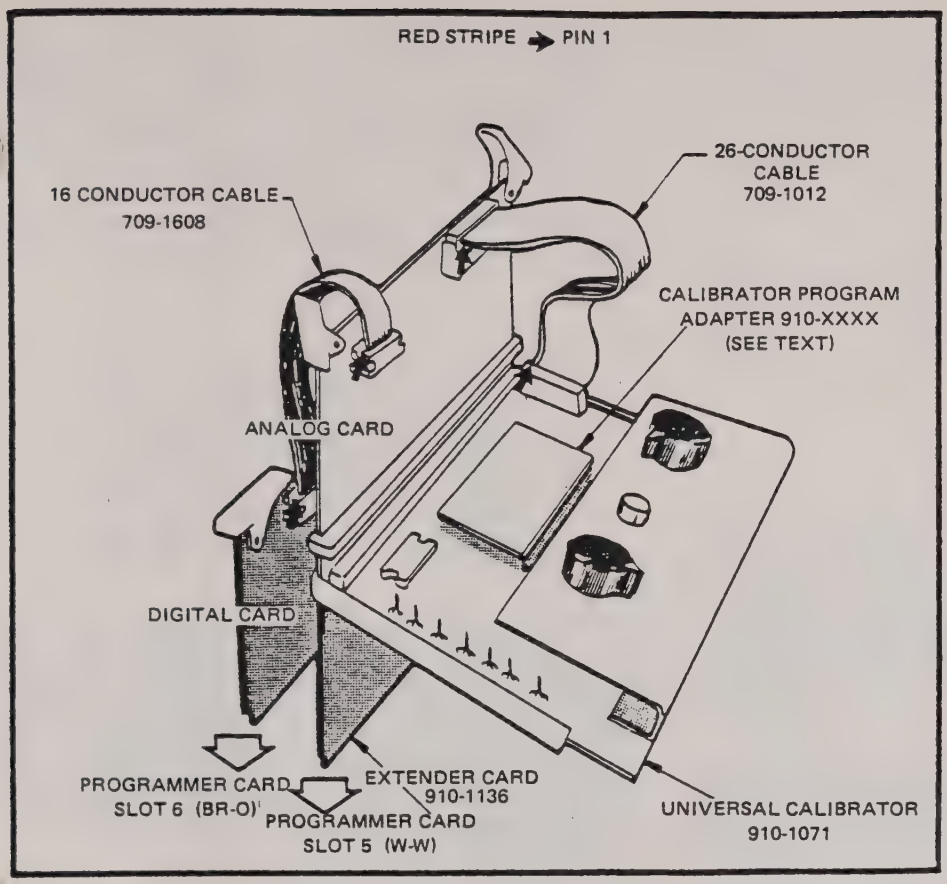


Figure 3. Installation of Universal Calibrator into Programmer Models 1, 2, 3, and 5 for AC Dynamic Tests.

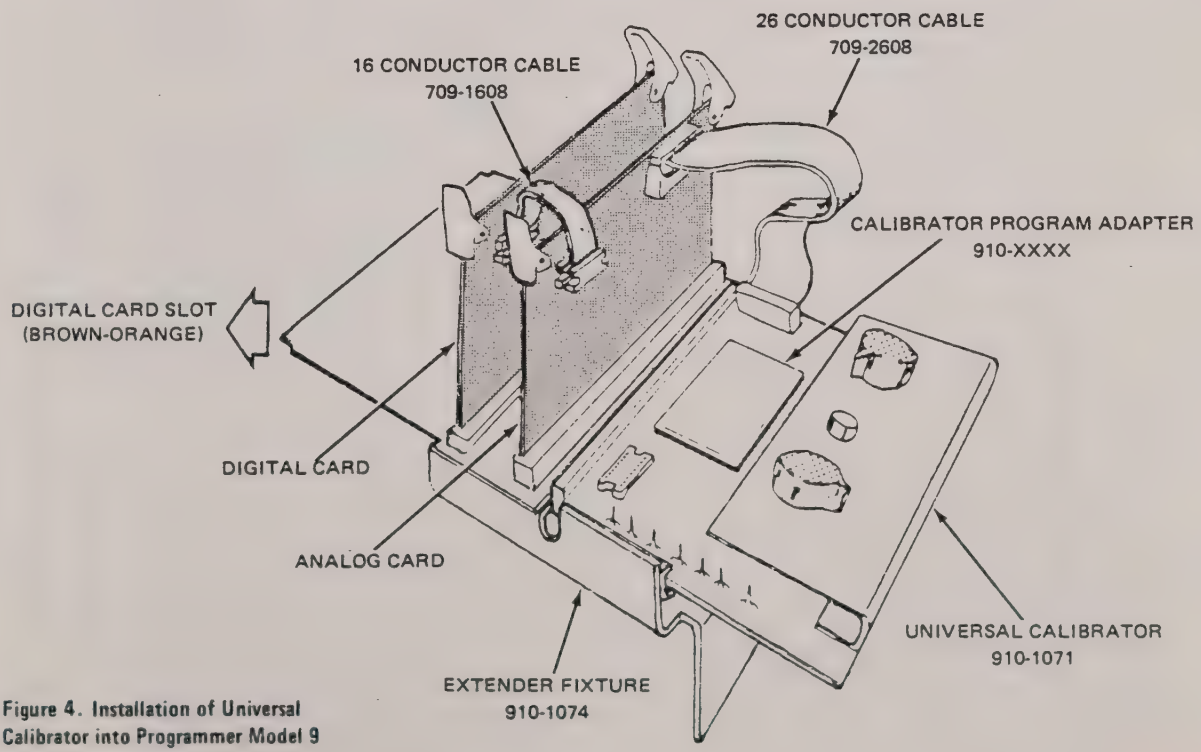


Figure 4. Installation of Universal Calibrator into Programmer Model 9 for AC Dynamic Tests.

10. Load approximately ten RAM addresses with bit 1 (only). This is accomplished by pressing 1 and FWD repetitively, or a tape may be used.

11. Programmers 1, 2, 3, 5:
Press: RESET
PROG
AUTO
RAM-ROM2

Programmer 9:
Press: PROGRAM

Waveform Observations

Initiate waveforms:
Programmers 1-5: press START.
Programmer 9: press EXECUTE.

The machine will stop on those addresses loaded in step 10 of the test set-up. If an abort condition is indicated, press WORD SKIP (SKIP on the Model 9) to advance the word count and repeat output of programming waveforms. An abort condition is indicated on Models 1, 2, 3, and 5 if the PROGRAMMING and INTERRUPT indicators come on. A Model 9 displays an abort condition by flashing the "P" indicator.

The "Program Waveforms" on the timing diagram at the rear of the manual are cross-referenced to the "Test Description" column on the Calibration Chart by circled digits (①, ②, ③, ...). To obtain the various waveforms use S2 and S3 on the Universal Calibrator to select the positions indicated in the "Switch Positions" column of the calibration chart and press S1 to test. S3 routes analog card output to TP3 (oscilloscope probe); S2 selects resistive loads, which are connected to ground when S1 is pressed.

NOTE: *All other information on the calibration charts is of no importance during waveform observations.*

CAUTION

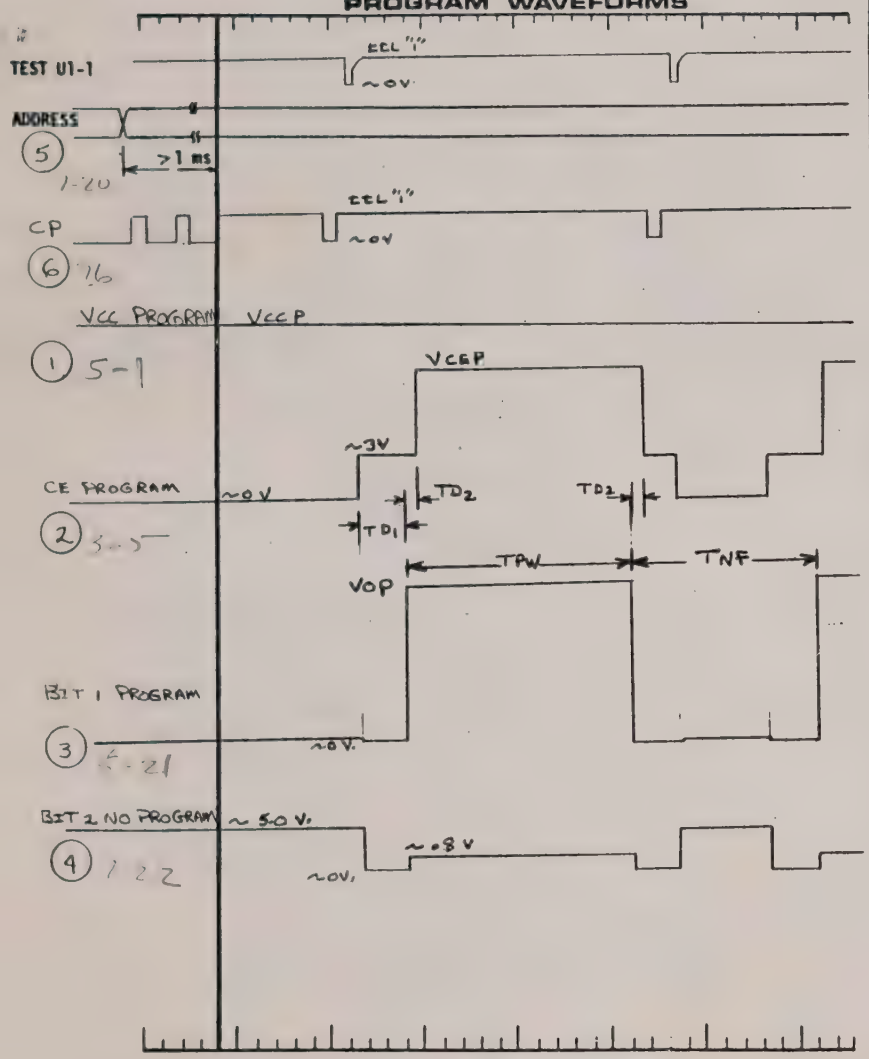
When S1 is pressed high currents are induced within the Programmer; do not hold S1 depressed for extended periods. High currents are also present when the programmer is locked into program mode with advanced word count; RESET before leaving programmer unattended during these tests.

During these tests note that the Abort, Pause, and Reject functions of the program card set remain active; Press WORD SKIP to refresh the display. The abort timer signals a reject after a specific programming time. The pause timer controls the on/off time of the programming function. The position of the reject jumper (C or M) limits the number of applied programming pulses. Refer to the notes column of the timing diagram for definitions of the abort, pause, and reject functions.

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
64	04	ADDRESS TEST A2 VIH	8-14	1365	555	2525	7	18	TP3		4.8		5.15
64	04	ADDRESS TEST A3 VIL	8-15	1365	555	2525	7	17	TP3		0.0		0.4
64	04	ADDRESS TEST A4 VIH	8-16	1365	555	2525	7	16	TP3		4.8		5.15
64	04	ADDRESS TEST A5 VIL	8-17	1365	555	2525	7	15	TP3		0.0		0.4
64	04	ADDRESS TEST A6 VIH	8-18	1365	555	2525	7	14	TP3		4.8		5.15
64	04	ADDRESS TEST A7 VIL	8-19	1365	555	2525	7	13	TP3		0.0		0.4
64	04	ADDRESS TEST A8 VIH	8-20	1365	555	2525	7	2	TP3		4.8		5.15
64	04	ADDRESS TEST A9 VIL	8-21	1365	555	2525	7	3	TP3		0.0		0.4
64	04	ADDRESS TEST A10 VIH	8-22	1365	555	2525	7	4	TP3		4.8		5.15
64	04	← DATA PATTERN FOR ALL WORDS NOT SHOWN											

CALIBRATION CHART 017-1286-1

PROGRAM WAVEFORMS



NOTES

FAST CLOCK = Adj. FOR TPW1
SLOW CLOCK = Adj. FOR TPW2

DIGITAL CARD JUMPERS
- JP1 = open
- JP2 = SHORT
- JP3 = SHORT
- JP4 = SHORT
- JP5 = SHORT
- JP6 = SHORT
- JP7C = 29 PULSE REJECT
- JP7M = NO REJECT
- JP8 = open
- JP9 = N
- JP10 = WORD LIMIT = 2048
- JP11 = SHORT

ABORT TIMER = NA

PAUSE TIMER (CR2) = OMIT

CLOCK RATE (CR7) = OMIT
CLOCK RATE (CR8) = LOAD

WAVEFORM VARIABLES

Vccp = 5.25 ± 0.25 V.
Vcc VL = 4.25±.25V
Vcc VH = 5.00±.25V
Vcc READ = 5.00±0.25V.

VCEP = 15.0 ±0.5 V.
VOP = 20.0±0.5V.

TD1 > 100 ns

TD2 > 100 ns
< 1 us

TNF < 20 us

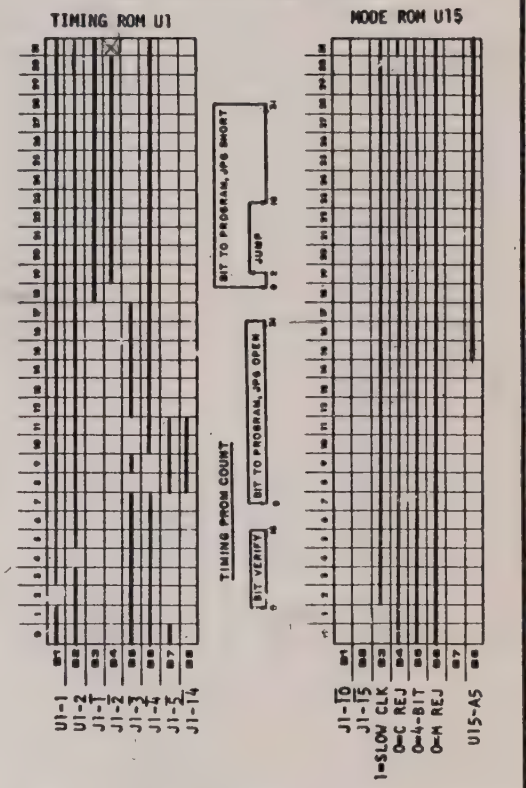
TPW = 50 ±5 us, Pulse #1
= 15 ±1.5 ns, Pulse 2-28

These waveforms correspond to callouts on the Calibration Chart. Switch S2 and S3 of the Universal Calibrator to indicated positions to obtain waveforms. Refer to Perfromance Check section of manual for detailed steps.

DATE	SYM	REVISION RECORD	DR.	CK.
11-2-77	C	RELEASE	GT	GT
4-3-78	D	ECN# 2308	KJ	X
7-3-78	E	ECN#2332	KJ	X
2-79	-	ECN #2594	FS	

TRUTH TABLES

LINE : HI(1); NO LINE : LOW(0)



DATA I/O ISSAQUAH, WASH.

TIMING DIAGRAM	DRAWN BY GT; APPROVED BY GT
TITLE: AMD GENERIC	
DATE: 11-2-77	DRAWING NUMBER: 007-1286-1

2/78

CIRCUIT DESCRIPTION

CIRCUIT DESCRIPTION, PROGRAM CARD SET

INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 4-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses from the analog card until either ABORT or REJECT is signaled, or until the bit is programmed.

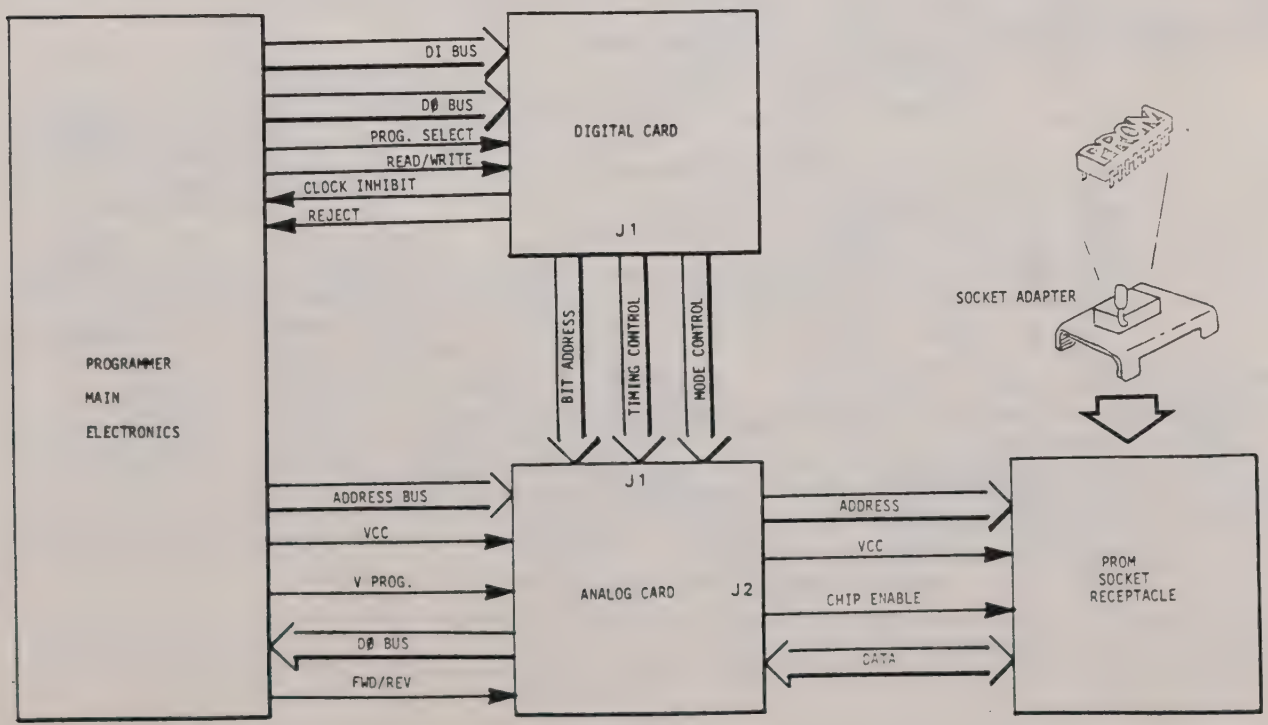
ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturer's specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow and timing. ROM truth tables, timing diagrams, jumper positions, and reject conditions are discussed. Detailed circuit schematics with timing diagrams and truth tables are found at the rear of this manual--refer to these for pin-out and interconnect information.

Fig. 4-1. Simplified Block Diagram of Program Card Set



BLOCK DIAGRAM

Figure 4-2 gives a generalized block diagram for the GP Digital Card. This diagram shows signal flow, and functional relationships between the blocks but does not include detailed interconnect information. Refer to the schematics and timing diagram (with truth tables) at the rear of this manual for details of circuit connection and operation. The following paragraphs discuss the functions contained on the digital card.

PROGRAM MEMORY

When the digital card is selected for operation, Program Memory will set upon receiving a Write command on AA. This causes the Clock Generator on the digital card to begin operation and halts the Programmer clock. Prior to setting of Program Memory, Program Pulse Counter, Bit Counter, and Sequence Counter are initialized, and Overprogram Counter is cleared.

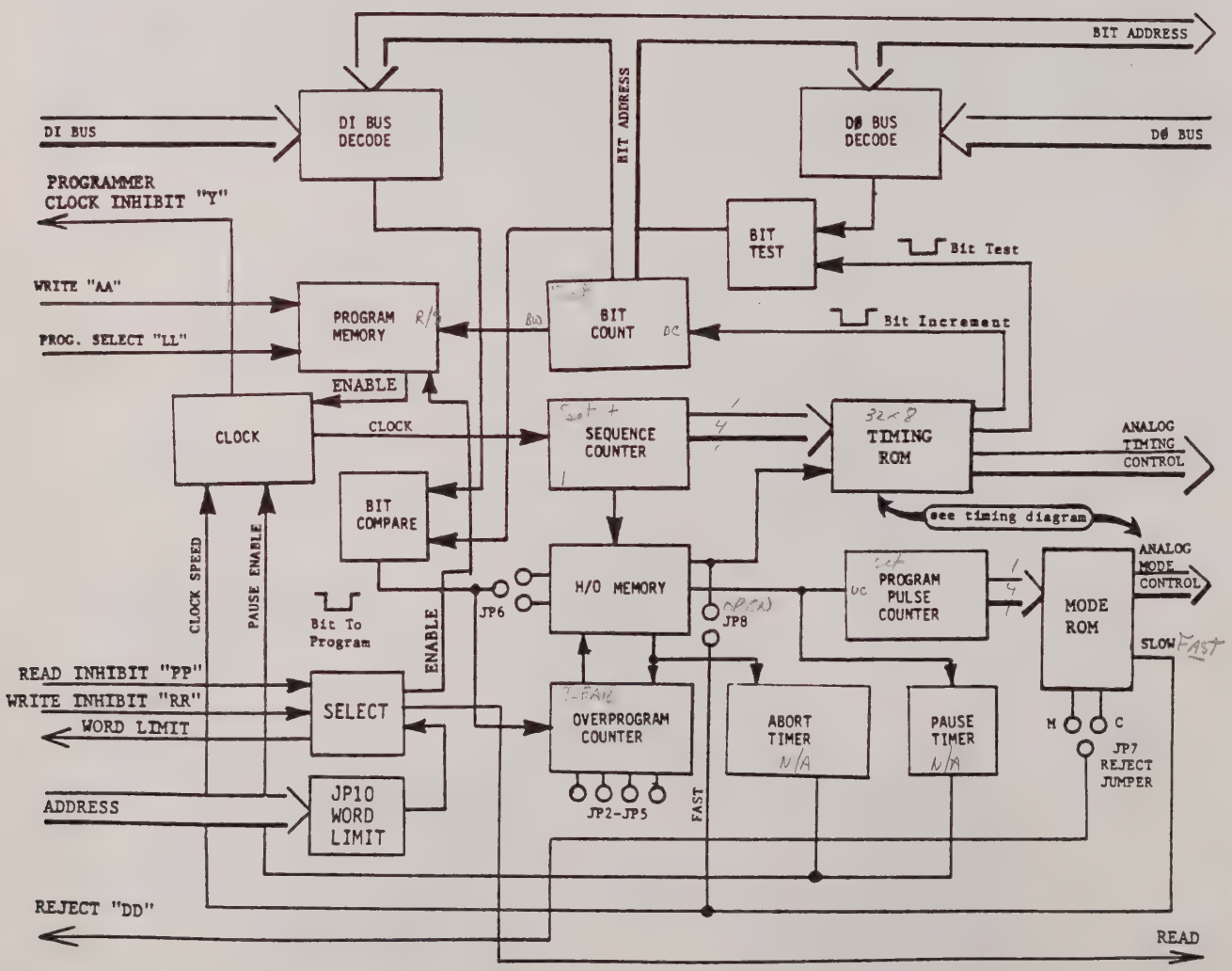
CLOCK GENERATOR

When Program Memory toggles in response to Write and Program Select commands, Clock Generator begins operation and the Programmer clock is inhibited. Clock pulses increment the Sequence Generator. Clock rate is determined by Mode and Timing ROM or by High Order Memory (with JP8 connected). The Clock may be halted by the Abort Timer, or by the Pause Timer (with CR2 connected).

SEQUENCE COUNTER AND TIMING PROM

The Sequence Generator consists of a 4-bit counter which drivers the 32x8 Timing ROM. The combination generates timing signals for analog control, along with Bit Test and Bit Increment pulses, which are used on the digital card (See Timing Diagram). A clock pulse is also output for PROMs with registers.

Fig. 4-2. Generalized Block Diagram for GP Digital Card



BIT COUNTER

The Bit Counter counts Bit Increment pulses arriving from the Timing ROM. Bit Increment pulses are counted, however, only when H/O Memory is enabled via a Bit to Program pulse from the Bit Compare gate. The Bit Counter counts down from either 4 or 8, as determined by input from the Analog Card or from the Mode ROM. Output from the Bit Counter controls the DO Bus Decoder and DI Bus Decoder. When the Bit Counter reaches zero, its borrow output is used to reset Program Memory.

PROGRAM PULSE COUNT AND MODE CONTROL

As program pulses are delivered to the PROM being programmed, the Program Pulse Counter counts up; outputs from the Program Pulse Counter are used as address line inputs to the Mode Control ROM. The Timing Diagram includes the truth table for the Mode Control ROM. Outputs of Mode ROM control the magnitude of program pulses (bits 1 and 2), along with clock speed (bit 3). Bits 4 and 5 control the number of programming attempts allowed before a reject is returned to the Programmer ; reject jumper JP7 selects either the M line or the C line (see Timing Diagram). M jumper sets the reject after one or more program attempts; C jumper rejects after multiple attempts, as determined in the Mode Control ROM.

TIMING PROM

Output words from the Timing ROM are used in the serial Verify and Program operations, as shown in the timing diagram. Verify operations utilize Low Order words 0 through 15; Program operations utilize High Order words 16 through 31. Words 8 through 11 are used to output control for Vcc voltages during Read and Verify operations. These operations occur under machine control when the digital card is not selected. At the beginning of a programming sequence (word 2), the Timing ROM outputs a Bit Test pulse to the Bit Test gate. If the DO Bus Decoder determines that there is no bit already programmed in the PROM, and if the DI Bus Decoder determines that there is a bit to program, then the Compare Gate outputs a Bit to Program pulse.

OVERPROGRAM COUNTER

The Bit to Program pulse arrives at the preset input of the H/O Memory, and at the load port of the Overprogram Counter. As H/O Memory is preset, the Bit Count Gate is disabled and remains so until the Overprogram Counter clocks H/O Memory after the bit has been programmed.

H/O MEMORY Word 15, the carry pulse from the Sequence Counter is allowed to toggle U13B (See Schematic). As U13B is toggled the fifth address line to the Timing ROM is enable, and it advances into High Order (Program) Count, words 16 through 31.

At word count 31, the Sequence Counter outputs another carry pulse to H/O Memory. The carry pulse toggles U13B, which sets the Timing ROM back to Low Order Count (Verify). At word 2, again, a Bit Test pulse is output from the Timing ROM; if the buses compare at Bit Test (bit is programmed), the output of Bit Compare gate remains unchanged (no Bit to Program), the H/O Memory remains enabled, and the Bit Count gate remains disabled.

At word 15 the Sequence Counter outputs another carry pulse which again causes High Order (Program) count, causing the Overprogram Counter to decrement. The above cycle repeats until the Overprogram Counter outputs a borrow pulse after counting down from the level preset by JP2-JP5. The borrow pulse clocks H/O Memory which enables the Bit Count gate, allowing it to decrement the Bit Count to the next bit.

Some digital cards are wired with JP6 shorted. If JP6 is shorted, Program Memory holds H/O Memory reset so that the Timing ROM jumps to High Order (Program Cycle) after Bit Test. When a Bit to Program pulse is received at (shorted) JP6, the fifth address input line to the Timing ROM goes high and H/O Memory is enabled. At Word 31, the carry pulse from the Sequence Counter shifts the count sequence back to Low Order. With JP6 shorted, the total sequence is 16 clock pulses long.

ABORT TIMER

The Abort Timer measures the time required to program a bit. If programming time is excessive, and JP1 is shorted, a REJECT is signaled and the clock is halted. The Abort Timer is connected to the Overprogram Counter such that an abort is possible only during Low Order count (Verify cycle).

PAUSE TIMER

The Pause Timer measures the time to program the PROM. A transistor is used in conjunction with the timing components to integrate out the time that the Program Memory is set. If programming time exceeds the value set by circuit components, the Clock is stopped in order to allow the PROM to cool; after a pause in the order of seconds the Clock is allowed to start again, and programming continues. Pause Timer output is gated with the Timing ROM so that a pause cannot occur during program pulses.

SELECT GATES

U17 and U18 (on schematic) monitor Program Select LL, Write Inhibit PP, Read X, and Read Inhibit RR in order to enable operation of the digital card. Output from Read Gate U17 is routed to the analog card to control the Data Bus Drivers.

WORD LIMIT SELECT

Word Limit is jumper-selected at JP10 on the digital card to 32, 64, 256, 512, 1024, or 2048. JP10 limits the address range of the Programmer through Word Limit line CC, according to the configuration of the PROM being programmed.

GENERAL DESCRIPTION—ANALOG

The 1286 Analog Card provides the drive requirements, sense amplifies and power supplies required to program the AMD Generic PROM family from the signals derived from the 1225 Digital Card.

GENERAL OPERATIONAL DESCRIPTION

The operation of the 1286 Analog card is as follows: First the device is addressed for a given word by the machine address lines through the Address Buffers. Then the appropriate program pulses are derived from signals received through J1 from the Digital Card and applied to the device through J2. Next, upon instructions from the Digital Card, the device is biased for the Read mode and the Comparators and Data Bus Drivers are enabled to transfer the data to the Output Bus. This cycle is repeated for each address where programmed bits are desired.

Each portion of the 1286 Analog Card is discussed below.

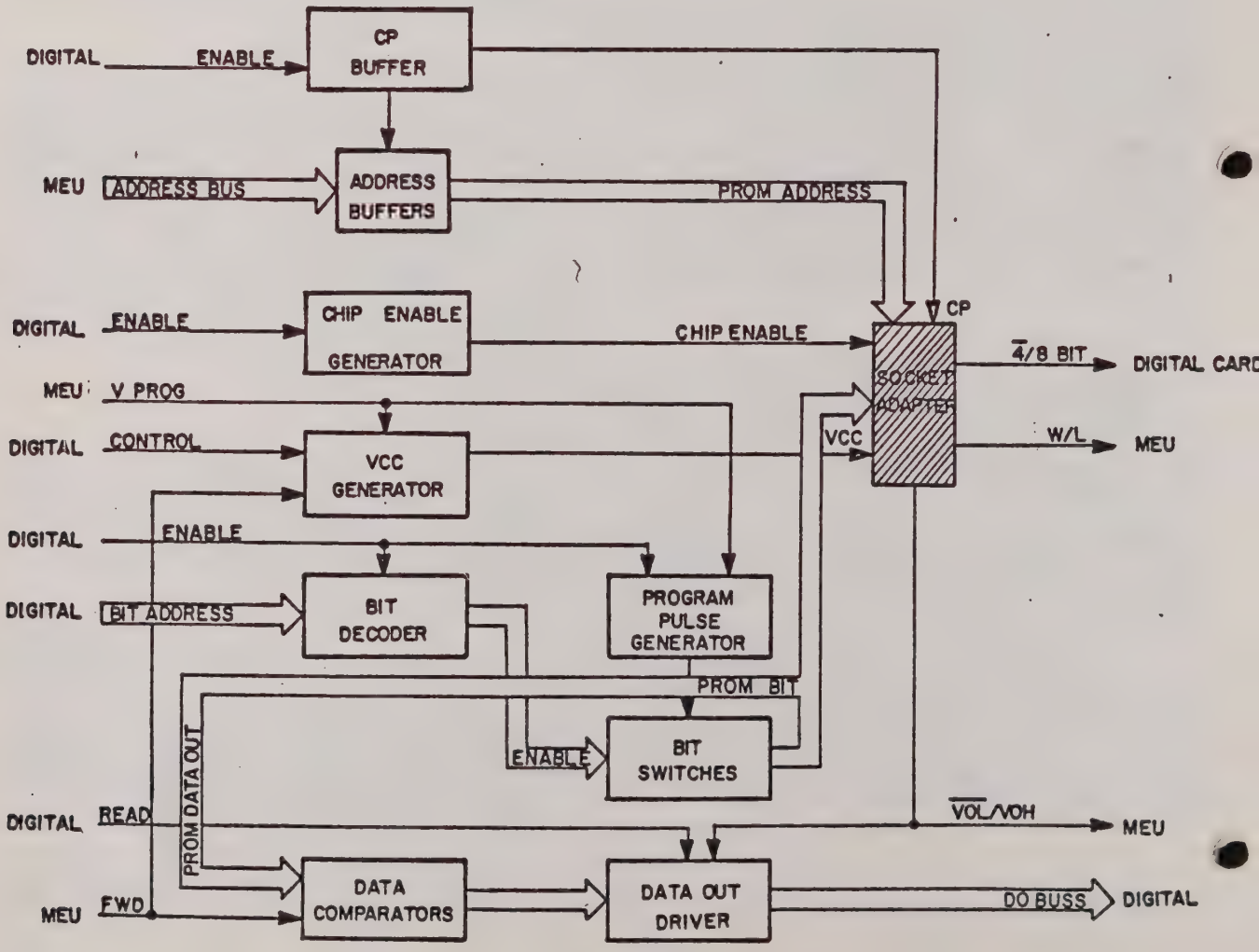
Address Buffers

The address signals from the Address Bus are buffered by a high voltage open collector 7407 (U13, U14) and applied to the appropriate device pins through J2.

Vcc Supply

The Vcc Supply consists of voltage regulator U5, a 723, and pass transistor Q10. The supply is killed during Stop by the action of the Start line, pin 22 on the edge connector. The various voltage levels during Read, Verify and Program are controlled via PROM U2. This PROM also controls loading of the PROM Bit Lines and controls comparator reference level.

Figure 4-3. Block Diagram Analog Card



Program Pulse Supply

The Program Supply consists of Darlington emitter follower Q14 and Q15 controlled by pin 4 of U3. The 741 U9 operates as an adjustable voltage clamp. When U9 goes high the base circuit capacitance of Q15 is charged from the + Prog. supply, then clamped at the required voltage by U9 to provide a fast rise time. Gate U3, pin 5 and 6, is included to provide a fast fall time. The reference voltage for the 741 is obtained from the internal 723 reference, pin 6 of U5. Zener diode CR16 and transistor Q13 perform the current limit function.

Chip Enable Pulse Supply

The chip enable supply consists of emitter follower Q1 controlled by Pin 2 of U3. As in the Program Pulse supply, a voltage clamp U8 is used to provide a fast rise time. Diode CR1 allows the CE to have three states OV, +5V supplied by pullup R33 and +15V supplied by Q1.

Bit Decoder

The Bit Decoder U4 is a 7445 device which receives its input from the Bit Counter on the Digital Card. The state of pin 12 of U4 controls the state of the particular output selected by the other three input lines.

Program Switch

The Program Switch consists of eight transistor switches Q2-Q9 connecting the Program-Pulse Supply to the various device bit outputs and driven from the Bit Decoder. The selected bit to program is connected to Program Pulse Supply Voltage. Unselected bits are held low during the program pulse.

Data Comparators

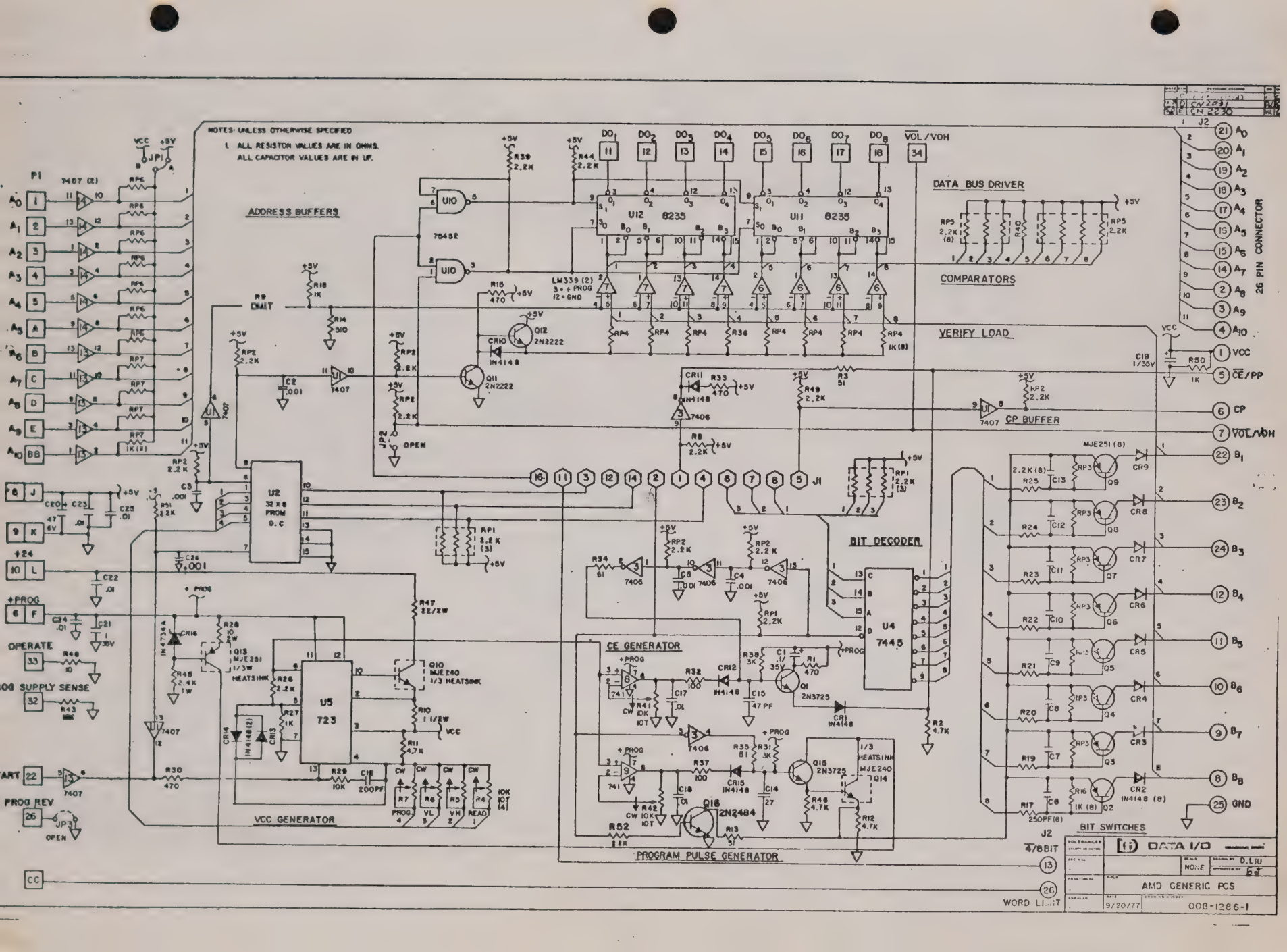
The bit lines from the device are connected to a 1K pullup, and to the non-inverting inputs of the LM 339 comparators U6 and U7. The inverting input is connected to a voltage reference source. Thus the variable compare level allows parametric testing of device VOL and VOH.

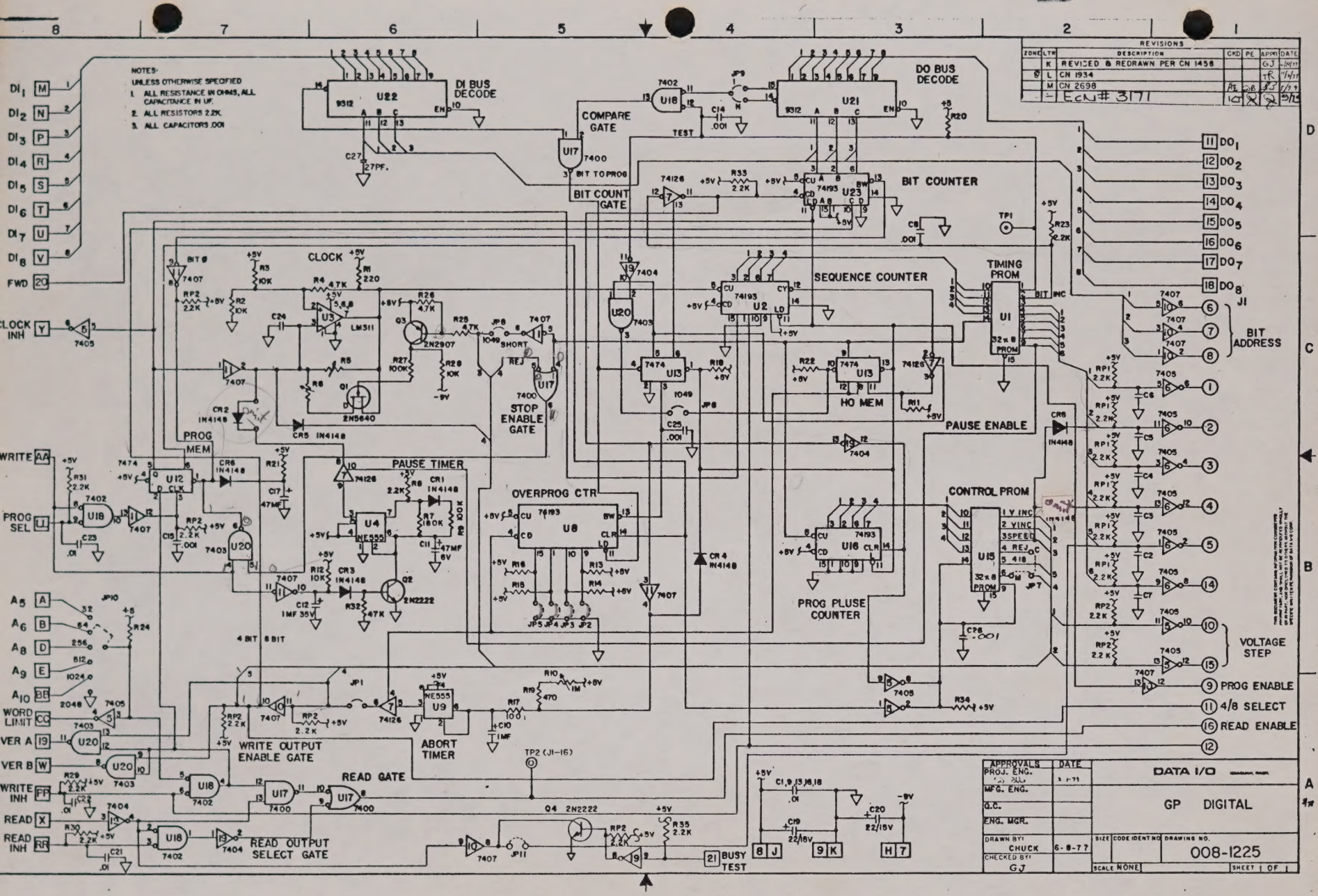
Data Bus Drivers

The output of the comparators is fed to 8235 Data Bus Drivers U11 and U12. The Data Bus Drivers are gated by a common line from the Digital Card so that device data is presented to the Bus at the correct time. The drivers also provide capability to invert the data on command from the socket adapter via pin 7 of J2. This allows for automatic data inversion for VOL or VOH devices.

CP Generator

The Clock Pulse (CP) Generator consists of gating U1 Pin 8 and 9 controlled by J1-5. Output from the generator is applied to the appropriate device pins through J2. This provides the necessary clocking required on PROM devices incorporating registers or latches.


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS.
ALL CAPACITOR VALUES ARE IN UF.
ADDRESS BUFFERS
DATA BUS DRIVER
COMPARATORS
VERIFY LOAD
CP BUFFER
BIT DECODER
CE GENERATOR
VCC GENERATOR
PROGRAM PULSE GENERATOR
BIT SWITCHES
26 PIN CONNECTOR
U2 32 X 8 PROM O.C
U4 7445
U5 723
U10 75432
U11 8235
U12 8235
LM339 (2) 3=+PROG 12=GND
OPERATE
+300 SUPPLY SENSE
PROG REV
WORD LIMIT
AMD GENERIC PCS
DATA I/O
9/20/77
008-1286-1
D.LIU


REVISIONS
ZONE LTR DESCRIPTION CKD PE APPR DATE
K REVISED & REDRAWN PER CN 1458 GJ 1/4/77
L CN 1934 TR 1/4/77
M CN 2698 GJ 5/5
ECN# 3171
NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE IN OHMS, ALL CAPACITANCE IN UF.
2. ALL RESISTORS 2.2K
3. ALL CAPACITORS .001
DI BUS DECODE
DO BUS DECODE
COMPARE GATE
BIT COUNT GATE
BIT COUNTER
SEQUENCE COUNTER
TIMING PROM
CLOCK
PROG MEM
PAUSE TIMER
OVERPROG CTR
HO MEM
PAUSE ENABLE
CONTROL PROM
PROG PLUSE COUNTER
STOP ENABLE GATE
WRITE OUTPUT ENABLE GATE
ABORT TIMER
READ GATE
READ OUTPUT SELECT GATE
BIT ADDRESS
VOLTAGE STEP
PROG ENABLE
4/8 SELECT
READ ENABLE
BUSY TEST
DI1 DI2 DI3 DI4 DI5 DI6 DI7 DI8
FWD
CLOCK INH
WRITE
PROG SEL
WORD LIMIT
VER A
VER B
WRITE INH
READ
READ INH
DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8
APPROVALS DATE
PROJ. ENG.
MFG. ENG.
Q.C.
ENG. MGR.
DRAWN BY CHUCK 6-8-77
CHECKED BY GJ
DATA I/O
GP DIGITAL
SIZE A CODE IDENT NO DRAWING NO. 008-1225
SCALE NONE SHEET 1 OF 1

DATA I/O

Programming systems for tomorrow... today